Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

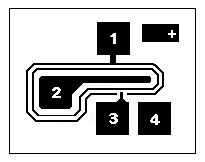
1. **SOURCE**
2. **DRAIN**
3. **GATE**
4. **DIODE**

**.022”**

**.019”**

**MASK**

**REF**



**SPI SD210-1B**

**2**

**4**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .0037” X .0037”**

**Backside Potential:**

**Mask Ref: SD210**

**APPROVED BY: DK DIE SIZE .019” X .021” DATE: 2/7/17**

**MFG: TELEDYNE / TOPAZ THICKNESS .011” P/N: SD211**

**DG 10.1.2**

#### Rev B, 7/19/02